PROCESS FOR MANUFACTURING A CHARGE-BALANCE POWER DIODE AND AN EDGE-TERMINATION STRUCTURE FOR A CHARGE-BALANCE SEMICONDUCTOR POWER DEVICE

PRIORITY CLAIM

[0001] This application claims priority from European patent application No. 06425448.5, filed Jun. 28, 2006, which is incorporated herein by reference.

TECHNICAL FIELD

[0002] An embodiment of the present invention relates to a process for manufacturing a bipolar power diode comprising charge-balance columnar structures, and relates to an edge-termination structure for a semiconductor power device, also comprising charge-balance columnar structures.

BACKGROUND

[0003] As is known, in the last few years a wide range of solutions has been developed for increasing the efficiency of semiconductor power devices, in particular in terms of increase in the breakdown voltage and decrease in the output resistance.

[0004] For example, U.S. Pat. Nos. 6,586,798, 6,228,719, 6,300,171 and 6,404,010, which are incorporated by reference, describe vertical-conduction semiconductor power devices, in which columnar structures of opposite conductivity are formed inside an epitaxial layer, forming part of a drain region having a given type of conductivity. The columnar structures have a dopant concentration which is substantially the same as, and of a type opposite to, the dopant concentration of the epitaxial layer in such a way as to provide a substantial charge balance (the so-called "Multi Drain (MD) technology"). The charge balance enables high breakdown voltages to be obtained, and moreover the high dopant concentration of the epitaxial layer enables a low output resistance (and low losses in conduction) to be achieved.

[0005] In brief, the formation of the aforesaid columnar structures envisages a sequence of steps of growth of N-type epitaxial layers, each step being followed by a step of implantation of a P-type dopant. The implanted regions are stacked so as to form the columnar structures. Next, body regions of the power device are formed in contact with the columnar structures, in such a manner that the columnar structures constitute an extension of the body regions into the drain region.

[0006] The evolution of this technology has witnessed a progressive increase in the density of the elementary strips forming the devices, for further increasing the charge concentration in the epitaxial layer and obtaining devices that, given the same breakdown voltage (which is substantially related to the height of the columnar structures), have a lower output resistance. On the other hand, however, the increase in the density of the elementary strips has led to a reduction of the thermal budget of the devices and a corresponding increase in the number of steps of epitaxial growth, and accordingly to an increase in the manufacturing costs and times, and in the defectiveness intrinsically linked to epitaxial growth.

[0007] Alternative technologies have consequently been developed to obtain charge-balance columnar structures; these technologies envisage, for example, formation of trenches inside the epitaxial layer and subsequent filling of the trenches with semiconductor material appropriately doped to obtain the charge balance.

[0008] For instance, in co-pending patent applications WO-PCTIT0600244, filed on Apr. 11, 2006, and WO-PC-TIT0600273, filed on Apr. 21, 2006, both in the name of the present applicant and incorporated by reference, improved techniques (which will in part be referred to in what follows) have been described for the formation of trenches and their filling, in particular substantially free from residual defectiveness, to obtain charge-balance structures, and for the formation of semiconductor power devices provided with the charge-balance structures. In particular, in WO-PC-TIT0600273 a non-selective epitaxial growth inside the trenches is proposed, also affecting a top surface of the layer in which the trenches are formed. Consequently, at the end of the epitaxial process a wrinkled surface layer made of semiconductor material may be formed, characterized by the presence of a plurality of grooves in areas corresponding to the columnar structures. It is also proposed to form the power devices at least in part inside this wrinkled surface layer.

[0009] Furthermore, as is known, the provision of efficient edge-termination structures is a key point for ensuring proper operation of power devices; in fact, it is in the edge areas that the largest number of breakdowns occur on account of the concentration of the electrical field lines due to the curvature of the edge regions. The edge terminations have the function of locally reducing the intensity of the electrical field so as to prevent peaks of intensity at the edges.

[0010] So far, the problem of providing edge-termination structures for charge-balance power devices, which enable maximization of the performance in reverse biasing of said devices, has not yet been solved in a satisfactory way for all applications.

SUMMARY

[0011] One or more embodiments of the present invention further improve the techniques for producing charge-balance power devices, in particular for the producing a bipolar power diode, and are directed to an efficient edge-termination structure for the aforesaid devices, based upon the power diode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] One or more embodiments of the invention are now described, purely by way of non-limiting example and with reference to the drawings, wherein:

[0013] FIG. **1** shows a cross section through a wafer made of semiconductor material in an initial step of a manufacturing process of a power diode and of a corresponding edge-termination structure, according to a first embodiment of the present invention;

[0014] FIG. **2** shows a top plan view of the wafer of FIG. **1** in a subsequent step of the manufacturing process;

[0015] FIGS. **3** to **10** show cross sections through the wafer of semiconductor material along the line of section III-III of FIG. **2**, in subsequent steps of the manufacturing process;

[0016] FIG. **11** shows a top plan view of a wafer of semiconductor material similar to that of FIG. **2**, corresponding to an embodiment of the present invention;

[0017] FIGS. **12** and **13** show cross sections through the wafer of semiconductor material along the line of section XII-XII of FIG. **11** in an initial step and in a final step of the manufacturing process, respectively;